AMENDMENTS TO THE CLAIMS

This listing of the claims replaces all prior versions, and listings, of the claims in the application.

LISTING OF THE CLAIMS

1-22. (Cancelled)

23. (Currently Amended) A memory device comprising at least a level shifter adapted to ~~standoff~~ stand off a high programming voltage to at least one fuse element in the memory device, wherein said high ~~programmable~~ programming voltage is used to set a state of the memory device.

24. (Previously Presented) The memory device of Claim 23 further comprising at least one storage element adapted to store data.

25. (Currently Amended) The memory device of Claim 23, wherein said level shifter comprises at least one PFet transistor adapted to ~~standoff~~ stand off said high voltage to at least one other PFet transistor in the memory device.

26. (Currently Amended) The memory device of Claim 23, wherein said level shifter comprises at least one NFET transistor adapted to ~~standoff~~ stand off said high voltage to at least one other NFet transistor in the memory device.

27. (Previously Presented) The memory device of Claim 23 further comprising a programming device adapted to set said state of the memory device.

28. (Previously Presented) The memory device of Claim 27, wherein said programming device comprises at least one switch transistor adapted to select at least a portion of said fuse element, enabling said high programming voltage to be communicated thereto.

29. (Previously Presented) The memory device of Claim 27, wherein said programming device comprises at least one transistor adapted to keep at least a portion of said fuse element low when setting said state of the memory device.

30. (Previously Presented) The memory device of Claim 23 wherein said fuse element comprises at least one gate-ox fuse adapted to selectively set said state of the memory device using said high programming voltage.

31. (Previously Presented) The memory device of Claim 30, wherein said gate-ox fuse comprises at least two coupled Nfet transistors.

32. (Previously Presented) The memory device of Claim 30, wherein said gate-ox fuse is a thin gate-ox fuse.

33. (Previously Presented) The memory device of Claim 32, wherein an oxide of said thin gate-ox fuse is about 2.5nm thick or less.

34. (Currently Amended) A memory device comprising at least a level shifter adapted to ~~standoff~~ stand off a programming voltage to at least one of two gated fuses in the memory device, wherein said programming voltage is used to set a state of the memory device.

35. (Previously Presented) The memory device of Claim 34 further comprising at least one storage element adapted to store data.

36. (Currently Amended) The memory device of Claim 34, wherein said level shifter comprises at least one PFet transistor adapted to ~~standoff~~ stand off said programming voltage to at least one other PFet transistor in the memory device.

37. (Currently Amended) The memory device of Claim 34, wherein said level shifter comprises at least one NFET transistor adapted to ~~standoff~~ stand off said programming voltage to at least one other NFet transistor in the memory device.

38. (Previously Presented) The memory device of Claim 34 further comprising a programming device adapted to set said state of the memory device.

39. (Previously Presented) The memory device of Claim 38, wherein said programming device comprises at least one switch transistor adapted to select at least a portion of at least one of said two gated fuses enabling said programming voltage to be communicated thereto.

40. (Previously Presented) The memory device of Claim 38, wherein said programming device comprises at least one transistor adapted to keep at least a portion of at least one of said two gated fuses low when setting said state of the memory device.

41. (Previously Presented) The memory device of Claim 34 wherein at least one of said two gated fuses is a gate-ox fuse.

42. (Previously Presented) The memory device of Claim 41, wherein said gate-ox fuse comprises at least two coupled Nfet transistors.

43. (Previously Presented) The memory device of Claim 41, wherein said gate-ox fuse is a thin gate-ox fuse.

44. (Previously Presented) The memory device of Claim 43, wherein an oxide of said thin gate-ox fuse is about 2.5nm thick or less.

45. (Currently Amended) A method of programming a memory device comprising:

selecting at least one fuse to be blown using a programming voltage; and

standing ~~of~~ off said programming voltage to at least one non-selected fuse.

46. (Previously Presented) The method of Claim 45 comprising using a level shifter having at least one Nfet transistor to stand off said programming voltage to at least one NFet transistor in the memory device.

47. (Previously Presented) The method of Claim 45 comprising using a level shifter having at least one PFet device to stand off said programming voltage to at least one PFet transistor in the memory device.

48. (Previously Presented) The method of Claim 45, wherein at least one of said selected and non-selected fuses is a gated fuse.

49. (Previously Presented) The method of Claim 48 wherein said gated fuse is a thin oxide gated fuse.

50. (Previously Presented) The method of Claim 49, wherein an oxide of said thin oxide gated fuse is about 2.5nm thick or less.